LAB EXERCISE 4.1 Minterm and Maxterm Truth Tables

Objectives

In this lab exercise you will learn the use of minterm and maxterm truth tables. You will also demonstrate the equivalence of the minterm and maxterm forms of a logic expression.

Materials

LD-2 Logic Designer

74LS08 Quad 2-Input AND

74LS11 Triple 3-Input AND

74LS32 Quad 2-Input OR

Jumper Wires
(See Figure 4-28 for IC pinouts.)

Procedure

1. The truth tables used in this book till now have been minterm truth tables. Logic equations can be directly written from these tables in the sum of products form. (See Figure 4-16)

$Y = AB$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	0

$Y = \overline{A}B + A\overline{B}$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

FIGURE 4-16. Examples of Minterm Truth Tables.

> NOTE
>
> The logic equation is the sum of the logic products which cause a true (1) output. A maxterm or product-of-sums form of a truth table can be created by inverting all entries of the corresponding minterm truth table. Logic equations for this function can be directly written from the maxterm truth table as the product of the sums which cause the output to be true (1). Two examples of maxterm truth tables are shown in Figure 4-17.

$Y = (A + B)(A + \bar{B})(\bar{A} + B)$

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

$Y = (A + B)(\bar{A} + \bar{B})$

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	1

FIGURE 4-17. Examples of Maxterm Truth Tables.

Most of the truth tables you will see are minterm tables; however, you should learn to convert to the maxterm form. The truth table for step one is:

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

Write the logic equation for this minterm truth table.

____

2. Insert a 74LS08 and 74LS04 in the breadboard of the LD-2. Wire the power (+5 VDC) and ground pins for the ICs.

3. Wire S1 to pin 1 of the 74LS04 and to L1. Wire pin 2 of the 74LS04 to pin 1 of the 74LS08. This is for the A input.

4. Wire S2 to L2 and pin 2 of the 74LS08. S2 will serve as the B input.

5. ~~[illegible]~~ This is the circuit output. → Wire L3 to pin 3 of the 74LS08

6. Turn ~~S1–S3~~ to OFF. Turn power ON. D1 should light.

7. S1 and S2 are the A and B inputs which can be observed on L1 and L2. Use S1, S2 and L3 to determine a truth table for this logic circuit. Record this truth table.

8. Form the maxterm truth table for the truth table in step 7. Write equations for this function in product of sums form.

9. Remove the circuit used in step 7. Insert a 74LS04, 74LS32 and 74LS11 into the LD-2 breadboard. Wire power and ground to these circuits.

10. Wire S1 to pin 1 of the 74LS04, pin 1 of the 74LS32 and L1. This is the A input.

11. Wire pin 2 of the 74LS04 to pins 5 and 9 of the 74LS32.

12. Wire S2 to pin 3 of the 74LS04, L2 and pins 2 and 4 of the 74LS32. This is the B input.

13. Wire pin 4 of the 74LS04 to pin 10 of the 74LS32.

14. Wire pins 3, 6 and 8 of the 74LS32 to pins 3,4 and 5 respectively on the 74LS11.

15. Wire pin 6 of the 74LS11 to L3. This allows monitoring the circuit output.

16. Turn all logic switches to OFF. Turn ON power. D1 should light.

17. S1 is A, S2 is B, and L3 is the logic circuit output. Use S1, S2, and L3 to construct a truth table for this circuit. Record the truth table here. Leave the circuit connected and answer the following questions.

Questions

1. Compare the truth tables from steps 7 and 17. What do you notice about them?

___

___

___

2. Draw schematic diagrams of the circuits that produced the truth tables in steps 7 and 17.

3. Which circuit better performs this logic function ? (step 7 or step 17 ?). Why ?

___

___

___

LAB EXERCISE 4.2 Simplifying Logic Circuits

Objectives

In this lab exercise you will study and apply techniques to reduce redundant logic elements in combinational logic circuits.

Materials

LD-2 Logic Designer

74LS04 Hex Inverter

74LS08 Quad 2-Input AND

74LS27 Triple 3-Input NOR

74LS32 Quad 2-Input OR

Jumper Wires
(Ref. Figure 4-28 for IC pinouts.)

Procedure

1. A truth table for a logic function is shown in Figure 4-18. From this truth table write the sum of products form of the logic equation represented by the truth table.

FIGURE 4-18. Truth Table for Lab Exercise 4.2.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

2. Insert a 74LS04, 74LS08 and 74LS27 into the LD-2 breadboard. Wire power and ground to these ICs.

3. Wire S1 to 74LS04 pin 1, 74LS08 pin 9 and L1. This is the A input.

4. Wire 74LS04 pin 2 to 74LS08 pins 1 and 4.

5. Wire S2 to pin 3 of the 74LS04, ~~pin 5 of the 74LS08~~, and ~~L2~~. ~~Wire 74LS04 pin 4~~ to 74LS08 pins 2 and 10. This is the B input.

6. Wire pins 2 [3], 6, and 8 of the 74LS08 to pins 3, 4, and 5 , respectively, of the 74LS27.

7. Wire pin 6 of the 74LS27 to pin 5 of the 74LS04. Wire pin 6 of the 74LS04 to L3. This is the circuit output.

8. The schematic for the circuit constructed is shown in Figure 4-19.

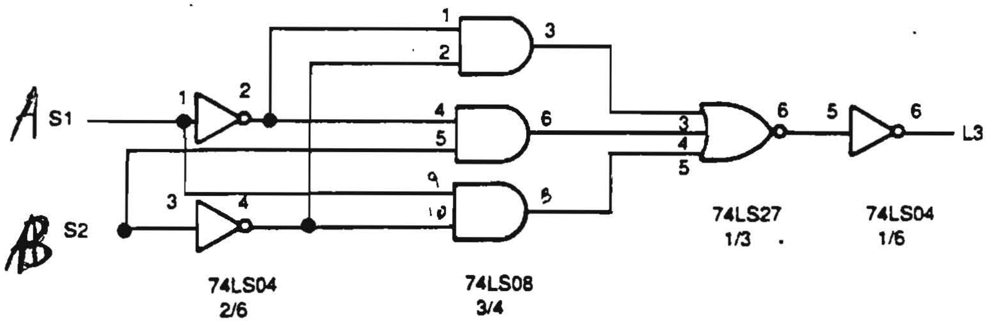


FIGURE 4-19. Step 7 Circuit Schematic.

9. Turn all logic switches to OFF. Turn ON poer. D1 and L3 should light.

10. Use S1, S2 and L3 to construct a truth table for this circuit. Record the truth table here.

11. This circuit has redundant elements. It could be converted to function the same with fewer components. We shall use Karnaugh maps to reduce the logic circuitry.

12. A generalized Karnaugh map for two variables is shown in Figure 4-20.

	$\bar{A}$	A
$\bar{B}$	$\bar{A}\bar{B}$	$A\bar{B}$
B	$\bar{A}B$	AB

FIGURE 4-20. Two Variable Karnaugh Map.

13. Use the truth table to fill the Karnaugh map with ones where appropriate. Form loops on the map. Record your results.

14. Write the simplified logic equation for this map here.

____

15. Remove the previous circuit from the breadboard. Put a 74LS04 and a 74LS32 onto the breadboard and wire power and ground to them.

16. Wire S1 to pin 1 of the 74LS04 and L1. Wire pin 2 of the 74LS04 to pin 1 of the 74LS32.

17. Wire S2 to pin 3 of the 74LS04 and L2. Wire pin 4 of the 74LS04 to pin 2 of the 74LS32.

18. Wire pin 3 of the 74LS32 to L3.

19. Turn all logic switches OFF and turn ON power. D1 and L3 should light.

20. S1 is A, S2 is B and L3 the circuit output. Use S1, S2 and L3 to construct a truth table for this circuit. Record your observations.

21. Leave this circuit connected while you answer the following questions.

Questions

1. What is the common name for the logic function displayed in the truth table in step 1?

____

2. What do you notice about the truth tables resulting from steps 10 and 20 ?

____

____

3. What do you call the simplified logic equation from the results of step 14 ?

____

4. Which of the circuits is better to use? Why?

____

____

____

LAB EXERCISE 4.3
Decoders

Objectives

You will learn about decoders in this lab exercise. You will study the simple decoder and the one of four decoder.

Materials

LD-2 Logic Designer

74LS04 Hex Inverter

74LS08 Quad 2-Input AND

74LS11 Triple 3-Input AND

Jumper Wires
(Ref. Figure 4-28 for IC pinouts.)

Procedure

1. The simple decoder will be studied first. A decoder detects the presence of a specific binary number or word. The decoder is usually formed from AND and NOT gates. Decoders are used extensively in computers for enabling memory and I/O devices.

2. Place a 74LS11 on the LD-2 breadboard. Wire the circuit shown. (See Figure 4-21)

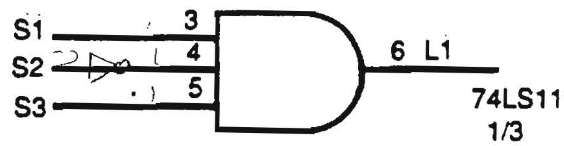


FIGURE 4-21. Schematic of a Simple Decoder.

3. Place all logic switches to OFF and apply power. D1 should light.

4. Use S1, S2, S3 and L1 to determine the truth table for this circuit. Record your observations here.

5. Turn off power and remove the circuit from step 4.

6. Place a 74LS04 and a 74LS08 on the LD-2 breadboard. Wire power and ground for these circuits.

7. Wire the circuit shown in Figure 4-22. This circuit is a one of four decoder.

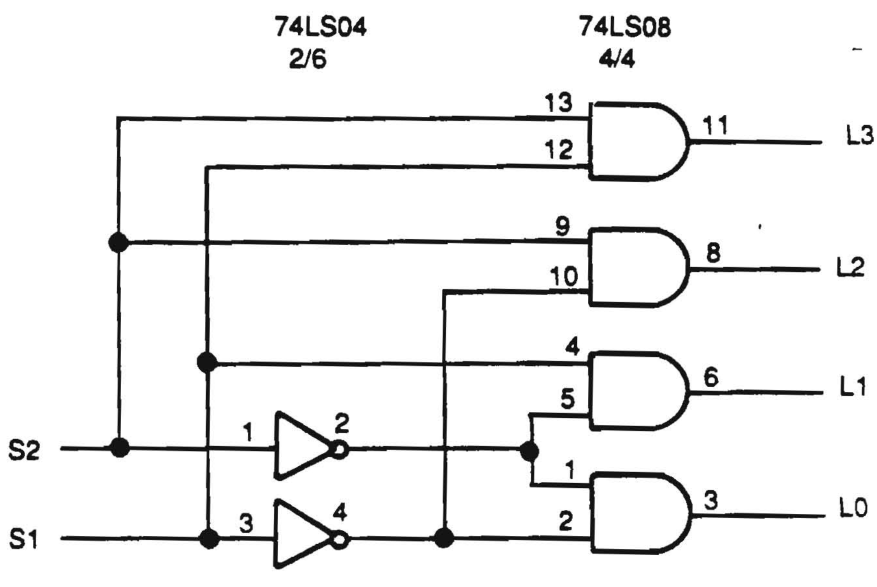


FIGURE 4-22. Schematic for a One of Four Decoder.

8. Turn the logic switches to OFF. Turn ON power. D1 and L0 should light.

9. Use S1, S2 and L0-L3 to form a table of the circuit operation.

10. Leave the circuit wired while you answer the following questions.

Questions

1. What binary number does the circuit form step 4 decode ?

____

2. Name one use of a circuit like the one in Figure 4-6.

____

3. Explain the operation of the one of four decoder.

____

____

____

4. Design a circuit to decode 101 binary.

5. Circuits similar to the one of four decoder are used to convert from BCD to decimal. How many AND gates will be required to implement such a circuit ? Hint: Examine Figure 4-22 schematic.

____

6. Why can't the logic equation from the truth table of step 9 be written as y = AB + AB + AB + AB ?

____

____

LAB EXERCISE 4.4 Encoders

Objectives

In this lab exercise encoders will be studied. Encoders accept one or more inputs and generate a mutli-bit binary output. You will study a simple encoder. The basic encoder circuit is the positive NAND gate.

Materials

LD-2 Logic Designer

74LS00 Quad 2-Input NAND

Jumper Wires
(Ref. Figure 4-28 for IC pinouts.)

Procedure

1. Wire the circuit shown in Figure 4-23. Note that PB1 and PB2, the LD-2 pushbuttons, have normally high and normally low connections.

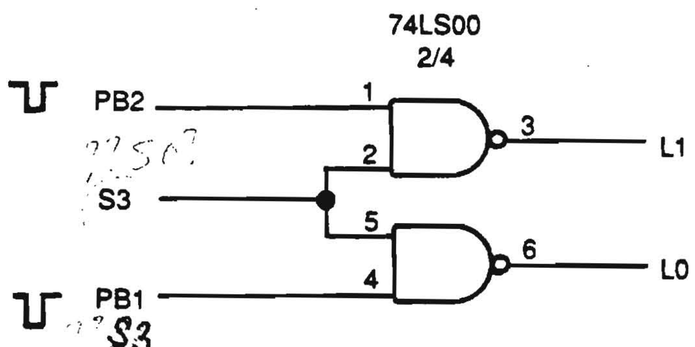


FIGURE 4-23. Schematic for a Simple Encoder.

2. Place S0 to ON. Turn on power. D1 should light.

3. Press PB1, PB2, and S3 one at a time. Note: S0 will have to be manually returned to ON. PB1 and PB2 return on their own.

4. Describe what happens when PB1 is pressed.

____

____

5. Record your observation when PB2 is pressed.

____

6. Place S0 to OFF. Record your observations.

____

7. Return S0 to ON.

8. Remove power from the circuit.

Questions

1. What does the circuit of step one do ?

____

____

LAB EXERCISE 4.5 Exclusive OR Circuits

Objectives

In this lab exercise the exclusive OR (EXOR) circuit and some applications of EXOR circuits will be studied.

Materials

LD-2 Logic Designer

74LS04 Hex Inverter

74LS08 Quad 2-Input NAND

74LS32 Quad 2-Input OR

74LS86 Quad EXOR

Jumpers
(Ref. Figure 4-28 for IC pinouts.)

Procedure

1. The truth table for the exclusive OR function is shown in Figure 4-24.

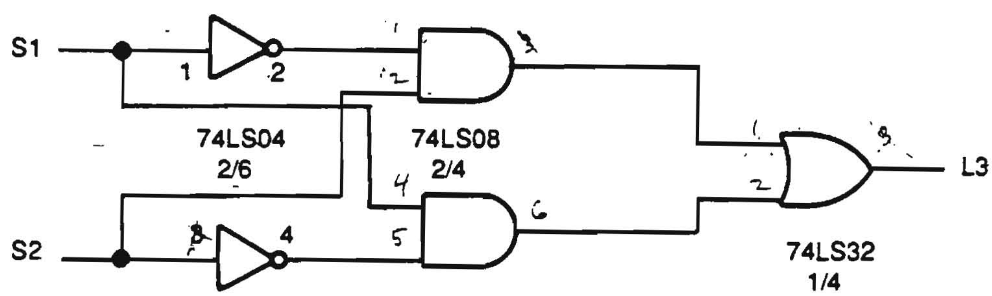
FIGURE 4-24. EXOR Truth Table.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

2. The logic expression for this truth table is $y = A\overline{B} + B\overline{A}$.

3. Wire a circuit from the schematic in Figure 4-25.

FIGURE 4-25. EXOR Schematic #1.



4. Place the logic switches OFF and turn ON power. D1 should light.

5. Use S1, S2 and L3 to form the truth table for this circuit. Record your observations here.

6. Notice that the circuit detects when the inputs are odd (not matched). For this reason, the EXOR is often called an odd/even detector.

7. Turn OFF power to the circuit. Remove the ICs from the breadboard.

8. Place a 74LS86 into the LD-2 breadboard.

9. Wire the circuit shown in Figure 4-26.

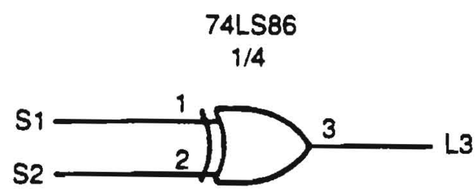


FIGURE 4-26. EXOR Schematic #2.

10. Turn logic switches OFF and power ON. D1 should light.

11. Use S1, S2 and L3 to form a truth table for this circuit. Record the truth table here.

12. You have focused on the logic circuit uses of the EXOR. The EXOR also performs a binary math function.

Questions

1. Examine the truth tables from steps 1, 5, and 11. What do you notice about them?

____

____

____

2. What math function does the EXOR gate perform ?

____

3. Which circuit is better to use, the one from step 3 or the one from step 9? Why?

____

____

4. Draw the Karnaugh map for the EXOR. Can this be reduced?

LAB EXERCISE 4.6
The EXNOR Circuit

Objectives

In this lab exercise the EXNOR circuit will be studied.

Materials

LD-2 Logic Designer

74LS04 Hex Inverter

74LS86 Quad EXOR

Procedure

1. Wire the circuit shown in the schematic of Figure 4-27.

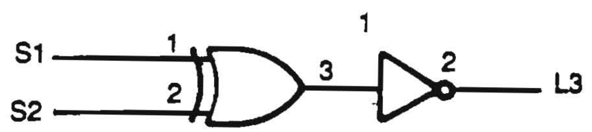


FIGURE 4-27. The EXNOR Circuit.

2. The EXNOR logic function is the complement of the EXOR.

3. Use S1, S2 and L3 to determine the truth table for this circuit. Record the truth table here.

4. Note that the EXNOR compares the value of A and B and outputs a 1 when the inputs are equal.

5. Remove the wire form S2 and wire it to PB1 normally high.

6. Operate S1 while observing L3. Record your observation.

____

Questions

1. Write the EXNOR logic equation directly from the truthtable.

____

2. What function does the circuit of step five perform ?

____

3. Make a Karnaugh map for the EXNOR function. Can this function be reduced ?